



Bit loading in mimo-plc systems with the presence of interference

Thanh Nhân Vo, Karine Amis Cavalec, Thierry Chonavel, Pierre Siohan

► To cite this version:

Thanh Nhân Vo, Karine Amis Cavalec, Thierry Chonavel, Pierre Siohan. Bit loading in mimo-plc systems with the presence of interference. EUSIPCO 2015: 23rd European Signal Processing Conference, Aug 2015, Nice, France. pp.904 - 908. hal-01214333

HAL Id: hal-01214333

<https://hal.science/hal-01214333>

Submitted on 13 Oct 2015

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Bit loading in MIMO-PLC systems with the presence of interference

Thanh Nhan VO¹, Karine AMIS¹, Thierry CHONAVEL¹, Pierre SIOHAN²
 1: Telecom Bretagne / UMR CNRS 6285 Lab-STICC; 2: Orange R&D Labs

Abstract—Power line has become attractive for data transmission thanks to its simple implementation that does not require any additional wires. Windowed orthogonal frequency division multiplex (OFDM) with adaptive bit loading has been selected to satisfy spectrum mask constraints of current regulations. In broadband indoor power line communication (PLC) systems, multiple input multiple output (MIMO) techniques have been introduced to address the increasing demand for high data rates under the constraint of limited allocated bandwidth. Whereas the self inter-antenna interference can be dealt with on each subcarrier, both inter-carrier and inter-symbol interference can occur yielding to sub-optimal bit loading if not considered. In this paper, we extend to the MIMO case the low-complexity bit/power allocation algorithm based on the Greedy principle and taking interference into account, that was first applied in the SISO case in our previous work, called Reduced Complexity Algorithm (RCA). Moreover, we also consider this problem for two cases: optimum eigen beamforming and spatial multiplexing. Simulation results show the efficiency of the RCA in terms of throughput and computation cost for both cases.

Index Terms—Bit-loading, Power allocation, MIMO, Interference, Power Line Communication, Greedy based approach.

I. INTRODUCTION

MIMO technique has been considered as a major key to increase the data rate in the next generation of broadband indoor power line communication systems. The HomePlug AV2 technology exploits the MIMO scheme to achieve higher data rates as well as a larger coverage [1]. MIMO-PLC is feasible since a protective earth (PE) wire is available in addition to phase (P) and neutral (N) wires. Hence, a scheme of MIMO with two transmitting antennas can be applied in the context of PLC. In interference-free OFDM systems, the bit loading problem is solved by the Water-filling algorithm [2], [3] for the continuous case and by Greedy based algorithms such as bit-adding and bit-removal [4], [5] for the discrete case. In SISO-OFDM systems with the presence of interference, the bit loading problem has been considered in [6], [7]. Recently, an efficient Greedy based approach has been proposed in [8] to solve the optimal bit/power allocation in SISO-PLC systems with the presence of interference resulting from an insufficient guard interval. Its achievable throughput is almost the same as the one obtained by the conventional Greedy approach. However, the complexity is significantly reduced.

In this paper, we consider the bit/power allocation problem for MIMO-PLC systems with the presence of inter-symbol and inter-carrier interference. The self inter-antenna interference is dealt with on each subcarrier. The key point is the transformation into an equivalent bit loading problem in SISO-PLC

systems and then the application of the reduced complexity approach in [8] with some small modifications involving power constraints to solve this problem.

The paper is organized as follows. In Section II, the bit loading problem in a 2x2 MIMO-PLC system with the presence of interference is introduced. In Section III, the transformation of this problem into an equivalent problem in SISO-PLC systems is shown. We then introduce the method of [8] to solve the problem for both cases: optimum eigen beamforming and spatial multiplexing. The simulation results and the complexity study are reported in Section IV. Finally, Section V is dedicated to conclusions and perspectives.

II. MIMO-PLC AND INTERFERENCE MODELS

In this paper, a 2x2 MIMO-PLC system is considered for the sake of simplicity. Let us consider a 2x2 MIMO-PLC system with L used subcarriers. On subcarrier m_0 , we have

$$\begin{bmatrix} y_1(m_0) \\ y_2(m_0) \end{bmatrix} = \begin{bmatrix} h_{11}(m_0) & h_{12}(m_0) \\ h_{21}(m_0) & h_{22}(m_0) \end{bmatrix} \begin{bmatrix} x_1(m_0) \\ x_2(m_0) \end{bmatrix} + \begin{bmatrix} I_{11}(m_0) + I_{12}(m_0) \\ I_{21}(m_0) + I_{22}(m_0) \end{bmatrix} + \begin{bmatrix} b_1(m_0) \\ b_2(m_0) \end{bmatrix} \quad (1)$$

where $y_j(m_0)$, $x_j(m_0)$ and $b_j(m_0)$ are the received signal, the transmitted signal and the Gaussian noise with variance $\sigma_j^2(m_0)$ at antenna j on subcarrier m_0 ; $h_{ji}(m_0)$ and $I_{ji}(m_0)$ are the channel frequency response and interference term from antenna i to antenna j on subcarrier m_0 .

Rewriting (1) under matrix form, we obtain

$$\mathbf{Y}(m_0) = \mathbf{H}(m_0)\mathbf{X}(m_0) + \mathbf{I}(m_0) + \mathbf{B}(m_0) \quad (2)$$

In SISO-PLC systems, the interference power on a given subcarrier depends on the signal power on all subcarriers [8], [9]. Similarly, the interference power in MIMO-PLC at a given receiver antenna and on a given subcarrier depends on the signal power at all antennas and on all subcarriers [10]. In [10], the covariance matrix of the noise plus interference $\mathbf{C}_{I+B}(m_0)$ has been written in the following form:

$$\mathbf{C}_{I+B}(m_0) = \begin{bmatrix} [\mathbf{W}_1\mathbf{P}](m_0) + \sigma_1^2(m_0) & [\mathbf{W}_2\mathbf{P}](m_0) \\ [\mathbf{W}_2^*\mathbf{P}](m_0) & [\mathbf{W}_3\mathbf{P}](m_0) + \sigma_2^2(m_0) \end{bmatrix} \quad (3)$$

where $\mathbf{P} = [P_1(1), \dots, P_1(L), P_2(1), \dots, P_2(L)]^T$ denotes the power allocation vector; \mathbf{W}_1 , \mathbf{W}_2 and \mathbf{W}_3 are the matrices of interference contributions, with size $L \times 2L$ (see [10] for more details about these matrices) and $[\mathbf{W}_i\mathbf{P}]$ is a vector with size $L \times 1$ resulting from the product of \mathbf{W}_i and \mathbf{P} .

In the following, to alleviate the notation, the subcarrier index m_0 is omitted. If the MIMO equalizer is based on zero-forcing (ZF), the detection matrix is given by

$$\mathbf{A} = \mathbf{H}^{-1} \quad (4)$$

Then, the signal of interest is

$$\mathbf{Z} = \mathbf{A}\mathbf{Y} = \mathbf{X} + \mathbf{A}(\mathbf{I} + \mathbf{B}) \quad (5)$$

Let us denote $\mathbf{A} = \begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix}$. The SINR level after ZF equalizer is

$$s_1 = \frac{P_1}{|a_{11}|^2[\mathbf{W}_1\mathbf{P}] + 2\Re(a_{12}^*a_{11}[\mathbf{W}_2\mathbf{P}]) + |a_{12}|^2[\mathbf{W}_3\mathbf{P}] + N_1}$$

$$s_2 = \frac{P_2}{|a_{21}|^2[\mathbf{W}_1\mathbf{P}] + 2\Re(a_{22}^*a_{21}[\mathbf{W}_2\mathbf{P}]) + |a_{22}|^2[\mathbf{W}_3\mathbf{P}] + N_2}$$

where $N_i = |a_{i1}|^2\sigma_1^2 + |a_{i2}|^2\sigma_2^2$.

The bit loading is done based on the SINR level:

$$b_i = \log_2 \left(1 + \frac{s_i}{\Gamma} \right), \quad b_i \in \mathcal{A}, \quad (i = 1, 2) \quad (6)$$

where \mathcal{A} denotes the set of allowable number of bits specified in IEEE P1901 standard [11], Γ is the SNR gap that models the practical modulation and coding scheme for a targeted symbol error rate: $\Gamma = \frac{1}{3} [Q^{-1}(\frac{SER}{4})]^2$, where SER is the target Symbol Error Rate and $Q^{-1}(x)$ is the inverse tail probability of the standard normal distribution [12].

A. Bit-power relation

The bit-power relations are in the form

$$P_1 = s_1 \left(|a_{11}|^2[\mathbf{W}_1\mathbf{P}] + 2\Re(a_{12}^*a_{11}[\mathbf{W}_2\mathbf{P}]) + |a_{12}|^2[\mathbf{W}_3\mathbf{P}] + N_1 \right) \quad (7)$$

$$P_2 = s_2 \left(|a_{21}|^2[\mathbf{W}_1\mathbf{P}] + 2\Re(a_{22}^*a_{21}[\mathbf{W}_2\mathbf{P}]) + |a_{22}|^2[\mathbf{W}_3\mathbf{P}] + N_2 \right) \quad (8)$$

where, using (6), $s_i = (2^{b_i} - 1)\Gamma$. We can see that the number of bits allocated to a given subcarrier depends not only on its power level but also on the power allocated to other subcarriers. Then, the bit-power relation problem is as follows:

Given a vector of number of bits \mathbf{b} allocated to the subcarriers and on the antennas, we have to find the corresponding vector of allocated power \mathbf{P} so that Eq.(6) is satisfied for all subcarriers.

B. Bit loading problem

The bit loading problem consists in finding the vector of allocated power that optimizes the achievable throughput. For 2x2 MIMO-PLC systems, it can be written as follows:

$$\begin{cases} \max_{\mathbf{P}} \sum_{m=1}^L \sum_{i=1}^2 b_i(m) \\ \sum_{m=1}^L \sum_{i=1}^2 P_i(m) \leq P_{tot} \\ \sum_{i=1}^2 P_i(m) \leq P_{max}(m) \end{cases} \quad (9)$$

This problem is quite difficult to solve because the number of bits allocated on any subcarrier depends on the power allocated on all subcarriers. Thus, we have to take into account the power allocated on all subcarriers to allocate the number of bits on any subcarrier. Fortunately, we addressed a similar problem in [8] for SISO-PLC systems. Hence, in this paper, we aim to transform the bit loading problem (9) into a problem equivalent to the case of SISO-PLC systems. Then, the reduced complexity approach in [8] can be reused with some small modifications to solve this problem.

III. BIT LOADING PROBLEM IN MIMO-PLC WITH THE PRESENCE OF INTERFERENCE

In this section, a solution of problem (9) is given. To this end, we transform it into an equivalent SISO problem. Let us consider the following notations

$$\mathbf{\Lambda} = \text{diag}(s_1(1), \dots, s_1(L), s_2(1), \dots, s_2(L)) \quad (10)$$

$$\mathbf{A}_1 = \text{diag}(|a_{11}(1)|^2, \dots, |a_{11}(L)|^2, |a_{21}(1)|^2, \dots, |a_{21}(L)|^2) \quad (11)$$

$$\mathbf{A}_2 = \text{diag}(a_{12}^*(1)a_{11}(1), \dots, a_{12}^*(L)a_{11}(L), a_{22}^*(1)a_{21}(1), \dots, a_{22}^*(L)a_{21}(L)) \quad (12)$$

$$\mathbf{A}_3 = \text{diag}(|a_{12}(1)|^2, \dots, |a_{12}(L)|^2, |a_{22}(1)|^2, \dots, |a_{22}(L)|^2) \quad (13)$$

$$\mathbf{W} = \mathbf{A}_1 \begin{bmatrix} \mathbf{W}_1 \\ \mathbf{W}_1 \end{bmatrix} + 2\Re \left(\mathbf{A}_2 \begin{bmatrix} \mathbf{W}_2 \\ \mathbf{W}_2 \end{bmatrix} \right) + \mathbf{A}_3 \begin{bmatrix} \mathbf{W}_3 \\ \mathbf{W}_3 \end{bmatrix} \quad (14)$$

$$\mathbf{N} = [N_1(1), \dots, N_1(L), N_2(1), \dots, N_2(L)]^T \quad (15)$$

Then, rewriting Eq. (7), (8) for all L subcarriers in a vector form, we obtain

$$\mathbf{P} = \mathbf{\Lambda}(\mathbf{W}\mathbf{P} + \mathbf{N}) \Rightarrow \mathbf{P} = (\mathbf{I}_{2L \times 2L} - \mathbf{\Lambda}\mathbf{W})^{-1} \mathbf{\Lambda}\mathbf{N} \quad (16)$$

Eq.(16) is the same as the one in [8] (c.f. Eq.(15)) except that the matrices are twice as big. Thus, we can extend the method obtained in the case of SISO-PLC in [8] with some slight modifications upon power constraints to solve the bit-loading problem for MIMO-PLC in the presence of interference. We recall that in the conventional Greedy algorithm, which is a popular tool for discrete optimization problems [13], at every iteration and for each subcarrier, we have to calculate the required power to increase throughput by one bit. Then, we choose the subcarrier that requires minimum power to increase after verifying the constraints of the total power allocated on every subcarrier and on all subcarriers remain satisfied. Eq.(16) shows that the computational complexity to calculate the power after increasing one bit on a subcarrier is that of a $2L \times 2L$ matrix inversion. Thus, the total complexity for one iteration in the conventional Greedy algorithm is the product of the number of subcarriers that can be loaded up and the complexity of a matrix inversion. Due to its important complexity, the conventional Greedy algorithm cannot be used in practical systems.

To reduce complexity, in [8] we have proposed the Reduced Complexity Algorithm (RCA). Its principle consists in the

simplification of the cost function (which is used to determine the subcarriers to increase number of bits) in the Greedy procedure and the use of a judicious initial bit vector instead of a null one as in the conventional Greedy approach and the efficient selection of K subcarriers to load up at every iteration. The main advantage of the RCA is that it almost converges to the same achievable throughput as the one obtained with the conventional Greedy algorithm. In addition, the RCA significantly outperforms the conventional Greedy algorithm in terms of complexity. For the sake of further complexity reduction, for the bit vector initialization, we use the Equal Power Allocation (EPA), i.e. the total power P_{tot} is identically allocated between the subcarriers and the antennas, instead of the Constant Power Water-Filling (CPWF) as in the original RCA in [8]. More details about the RCA can be found in [8].

Algorithm	Complexity per iteration	Number of iterations	Number of matrix inversions
Standard GR	$\approx \mathcal{O}(\beta U^4)$	N_s	$N_s * \mathcal{O}(\beta U)$
GR + Init	$\approx \mathcal{O}(4\beta_1 U^3)$	$N_1 \ll N_s$	$N_1 * \mathcal{O}(4\beta_1)$
RCA	$\approx \mathcal{O}(U^3)$	$N_K \ll N_s$	$N_K * \mathcal{O}(1)$

Table 1. Complexity per iteration, number of iterations and equivalent total number of matrix inversions.

The complexity comparison between the conventional Greedy, the Greedy with EPA initialized bit vector and the reduced complexity algorithms is illustrated in Table 1 where $1 \ll \beta_1 < \beta$, U is the length of the power vector \mathbf{P} and N_s , N_1 , N_K are the total number of iterations used in the standard Greedy algorithm, the Greedy algorithm with the EPA initialized bit vector and RCA respectively. In SISO systems, U is equal to L , the number of active subcarriers. In 2x2 MIMO systems, U is equal to $2L$. For more details about how to calculate the complexity of the algorithms, interested readers can refer to [8]. We can see that the RCA reduces not only the number of iterations but also the computation cost per iteration, due to the decrease of the average number of subcarriers for which we have to calculate the value of the cost function in the Greedy procedure.

In the following, we consider the bit/power allocation problem in MIMO-PLC systems with the presence of interference for the cases of optimum eigen beamforming and of spatial multiplexing. Indeed, we can use the proposed solution in section III to solve the problem in both cases. However, we have to change the detection matrix \mathbf{A} . We give here the formula to calculate \mathbf{A} in both cases.

A. Optimum eigen beamforming

In this case, the eigen beamforming is used as it offers a good performance by adapting the transmission in an optimum way to the underlying eigen modes of the MIMO-PLC channel. The underlying MIMO streams are obtained by a Singular Value Decomposition (SVD) of the channel matrix [14]

$$\mathbf{H} = \mathbf{U}\mathbf{D}\mathbf{V}^H \quad (17)$$

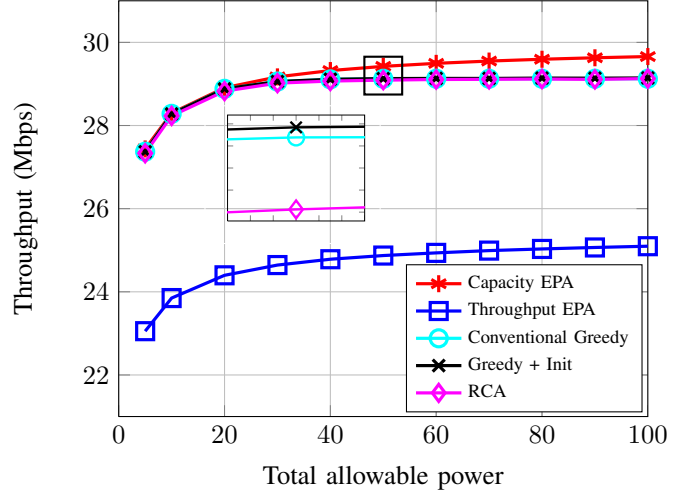


Fig. 1: Achievable throughput of different algorithms with spatial multiplexing.

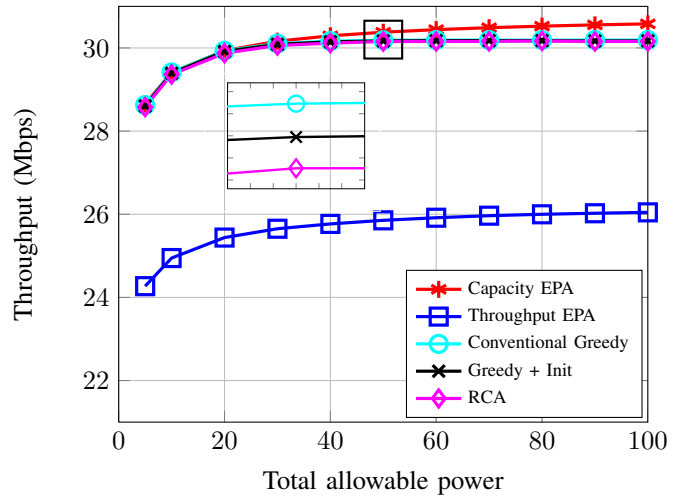


Fig. 2: Achievable throughput of different algorithms with optimum eigen beamforming.

where \mathbf{U} , \mathbf{V} are unitary matrices, i.e. $\mathbf{U}^{-1} = \mathbf{U}^H$ and $\mathbf{V}^{-1} = \mathbf{V}^H$, H denotes the Hermitian operator and \mathbf{D} is a diagonal matrix containing the single values of \mathbf{H} .

In the case of eigen beamforming with precoding matrix \mathbf{V} , the channel matrix \mathbf{H} is replaced by $\mathbf{H}\mathbf{V}$ in (2). Then, the detection matrix \mathbf{A} can be expressed as [1]

$$\mathbf{A} = (\mathbf{H}\mathbf{V})^{-1} = \mathbf{D}^{-1}\mathbf{U}^H. \quad (18)$$

B. Spatial multiplexing

In this case, no precoding is done and then the detection matrix is $\mathbf{A} = \mathbf{H}^{-1}$.

IV. SIMULATION RESULTS

The simulation parameters are the following:

- Exploitable subcarriers defined in the IEEE P1901 standard [11] with sampling rate $f_s = 100$ MHz, frequency shift $\Delta f = 24.414$ kHz.

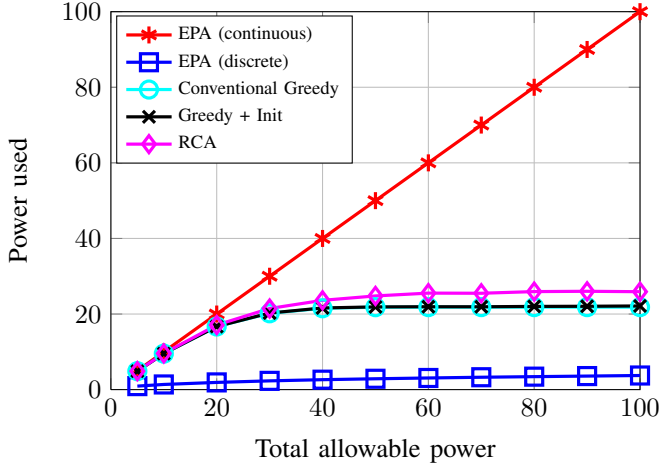


Fig. 3: Total consumed power of different algorithms with spatial multiplexing.

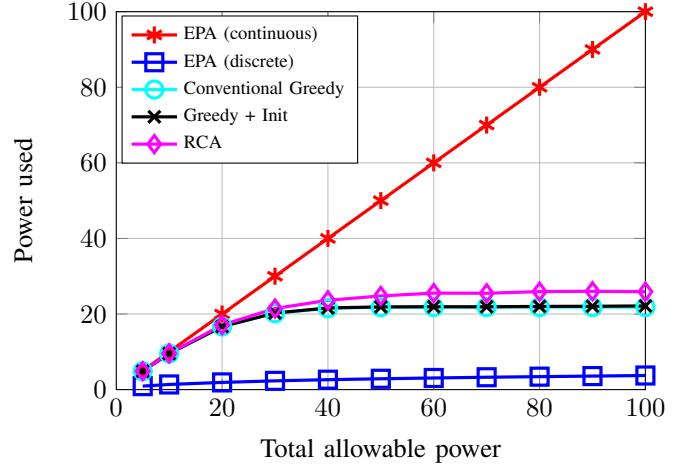


Fig. 4: Total consumed power of different algorithms with optimum eigen beamforming.

- Channel model: SISO-PLC Class 2 channel of Tonello's model [15] and 2x2 MIMO-PLC (same circuit using P-N, N-PE) of Hashmat model [16].
- Noise model: 2x2 MIMO-PLC independent noise of Esmailian model [17].
- Spectral mask constraint: $P_1(m) + P_2(m) \leq P_0$, $\forall m$. The total power allocated on any subcarrier is less than P_0 , where $P_0 = -50$ dBm/Hz [11].
- $\mathcal{A} = \{1, 2, 3, 4, 6, 8, 10, 12\}$ (bits).
- Number of channel realizations: 1000.

For the sake of simplicity, we only take into account the first 100 useful subcarriers out of 917 defined in IEEE 1901 standard in our simulation, i.e. $L = 100$. The calculation of covariance matrix \mathbf{C}_{I+B} is completely based on the calculation in [10] with the value of guard interval of $5.56 \mu s$, the minimum allowable value defined in the IEEE P1901 standard. In this case, the effect of interference on the system performance is significant. We illustrate in Figures 1 and 3 the achieved throughput and the power used with the EPA (in both cases: continuous bit-loading and discrete bit-loading), the conventional Greedy algorithm (GR), the Greedy with judicious initial bit vector (GR + Init) and the RCA, respectively in the case of spatial multiplexing. Figures 2 and 4 supply the same informations in the case of optimum eigen beamforming. In the RCA, the number of subcarriers chosen to simultaneously increase the number of bits is set to 5.

Algorithm	Throughput (Mbits)	Number of inversions	Run-time (s)
EPA (continuous)	29.42	–	–
Standard GR	29.12	1070	17.2
GR + Init	29.13	207	2.7
RCA	29.09	38	0.5
EPA (discrete)	24.90	–	–

Table 2. Throughput and run-time comparison between different algorithms with spatial multiplexing.

For both cases, the performance of GR, GR + Init algorithms in terms of achievable throughput is almost the same. The

achievable throughput of the proposed RCA is little degraded when compared to that obtained with the GR algorithms and significantly improved as compared to the EPA algorithm. The maximal shift of achievable throughput between RCA and the conventional GR is about 0.2% and in average, the RCA increases the achievable throughput by 17% w.r.t the EPA algorithm in both cases. In addition, we can see that the achievable throughput obtained by the RCA with optimum eigen beamforming is increased by about 4% (in average) as compared to the one of spatial multiplexing. Hence, as compared to the spatial multiplexing, the achievable throughput gain obtained by the optimum eigen beamforming is not really significant in 2x2 MIMO-PLC systems with significant interference resulting from an insufficient guard interval. The achievable throughput comparison when the total normalized power $P_{tot} = 50$ and with spatial multiplexing is shown in Table 2.

Figure 5 shows the complexity of different algorithms that is represented by the total number of matrix inversions used to find the bit/power allocation in the case of spatial multiplexing. Note that the vertical axis is in logarithmic scale. The complexity of different algorithms with optimum eigen beamforming is almost the same when compared to the one illustrated in Figure 5. For both cases, the RCA has reduced the complexity by 97% as compared to the conventional GR algorithm. However, as mentioned above, the achievable throughput for both algorithms is almost the same. The run-time comparison when $P_{tot} = 50$ is also shown in Table 2. As compared to the conventional Greedy algorithm, the RCA only degrades the achievable throughput by 0.1%. However, the run-time is reduced by about 35 times. It is shown that the RCA is efficient to solve the bit/power allocation in MIMO-PLC systems with the presence of interference.

V. CONCLUSION

In this paper, we have extended the Reduced Complexity Algorithm (RCA) for the problem of achievable throughput maximization in SISO-PLC systems to MIMO-PLC systems

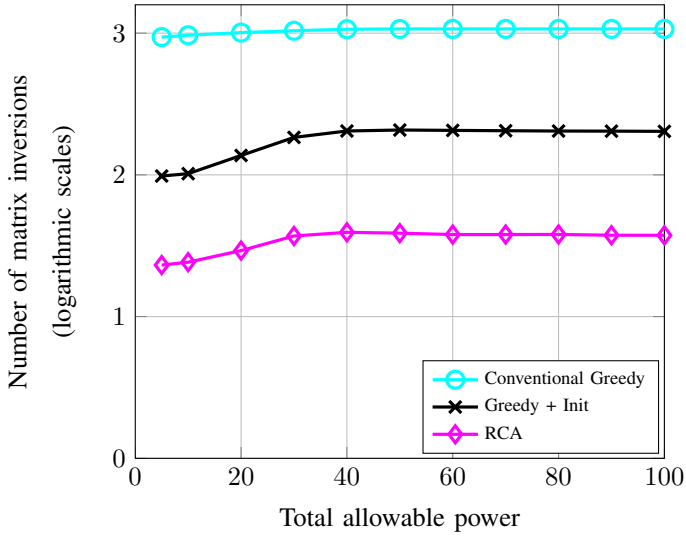


Fig. 5: Complexity of different algorithms with spatial multiplexing.

in presence of interference. To this end, we have transformed the MIMO-PLC problem into an equivalent SISO-PLC problem. Simulation results have clearly shown that the reduced complexity algorithm is also efficient for the problem of achievable throughput maximization in MIMO-PLC systems in presence of interference, i.e. the achievable throughput loss is negligible and the complexity is significantly reduced as compared to the Greedy solutions. It is also shown that the RCA algorithm outperforms the EPA algorithm. Therefore, it is a good candidate to solve resource management problems for single-user Windowed-OFDM systems in the presence of significant interference for both SISO and MIMO systems. Our future work aims to solve the bit/power allocation problem for the multi-user with/without the presence of interference in SISO/MIMO-OFDM systems.

REFERENCES

- [1] L. Yong and al., "An overview of the HomePlug AV 2 technology," *Journal of Electrical and Computer Engineering*, 2013.
- [2] E. Baccarelli, A. Fasano, and M. Biagi, "Novel efficient bit-loading algorithms for peak-energy-limited ADSL-Type multicarrier systems," *IEEE Transactions on Signal Processing*, vol. 50(5), pp. 1237–1247, 2002.
- [3] N. Papandreou and T. Antonakopoulos, "Bit and power allocation in constrained multicarrier systems: The single-user case," *EURASIP Journal on Advances in Signal Processing*, 2008.
- [4] W. Al-Hanafy and S. Weiss, "A new low-cost discrete bit loading using greedy power allocation," *Mosharaka International Conference on Communications, Computers and Applications*, 2009.
- [5] N. Papandreou and T. Antonakopoulos, "A new computationally efficient discrete bit-loading algorithm for DMT applications," *IEEE Transactions on Communications*, vol. 53(5), pp. 785–789, 2006.
- [6] J.-H. Wen, C.-H. Chiang, T.-J. Hsu, and H.-L. Hung, "Resource management techniques for OFDM systems with the presence of inter-carrier interference," *Wireless Personal Communication*, vol. 65(3), pp. 515–535, 2011.

- [7] M. K. Chan and W. Yu, "Multiuser spectrum optimization for discrete multitone systems with asynchronous crosstalk," *IEEE Transactions on Signal Processing*, vol. 55(11), pp. 5425–5435, 2007.
- [8] T. N. Vo, K. Amis, T. Chonavel, and P. Siohan, "Achievable Throughput Optimization in OFDM Systems in the Presence of Interference and its Application to Power Line Networks," *IEEE Transactions on Communications*, vol. 62(5), pp. 1704 – 1715, 2014.
- [9] P. Achaichia, M. L. Bot, and P. Siohan, "OFDM/OQAM: A solution to efficiently increase the capacity of future PLC networks," *IEEE Transactions on Power Delivery*, vol. 26(4), pp. 2443–2455, 2011.
- [10] T. N. Vo, K. Amis, T. Chonavel, P. Siohan, and P. Pagani, "Influence of Interference in MIMO Power Line Communication systems," *IEEE ISPLC*, pp. 255–260, 2014.
- [11] I. C. Society, *IEEE Standard for Broadband over Power Line Networks: Medium Access Control and Physical Layer Specification*, 2010.
- [12] J. M. Cioffi, *A multicarrier prime*. [Online]. Available: <http://www.stanford.edu/group/cioffi/publications.html>
- [13] H. Cormen, E. Leiserson, L. Rivest, and C. Stein, *Introduction to Algorithms*. MIT Press, 2001.
- [14] A. Paulraj, R. Nabar, D. Schill, and D. Gore, *Introduction to Space-Time Wireless Communications*. Cambridge University Press, 2003.
- [15] M. Tonello, F. Versolatto, B. Bejar, and S. Zazo, "A fitting algorithm for random modeling the PLC channel," *IEEE Transactions on Power Delivery*, vol. 27(3), pp. 1477–1484, 2012.
- [16] R. Hashmat, P. Pagani, Z. A., and T. Chonavel, "A channel model for multi input multi output in-home power line networks," *IEEE ISPLC 2011*, pp. 35–41, 2011.
- [17] R. Hashmat, P. Pagani, and T. Chonavel, "Analysis and modeling of background noise for inhome MIMO-PLC channels," *IEEE ISPLC 2012*, pp. 316–321, 2012.